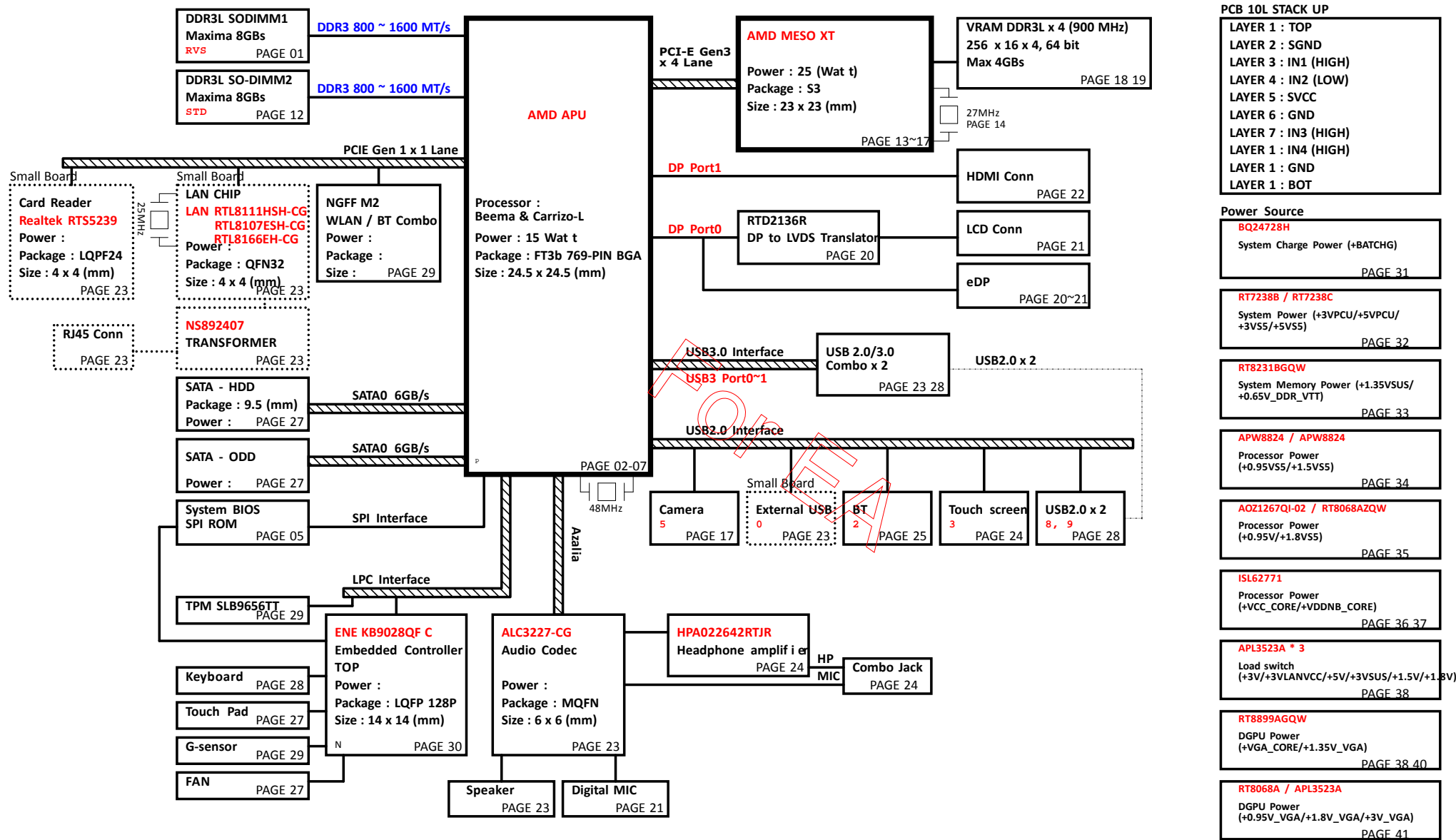


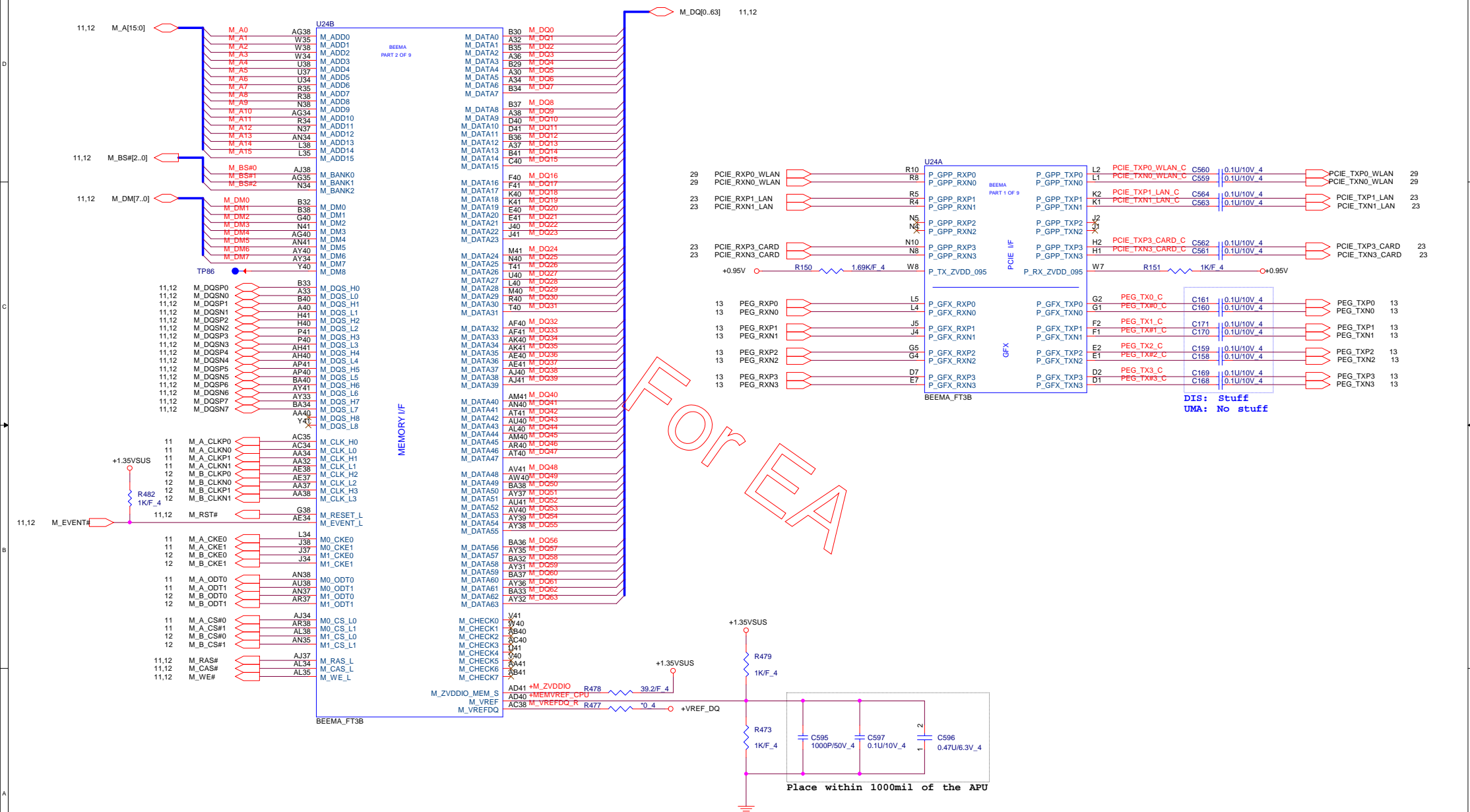
Chocolate AMD Beema DIS/UMA (14.0"/15.6"/17.3")

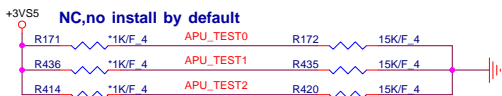


PROJECT : X22
Quanta Computer Inc.

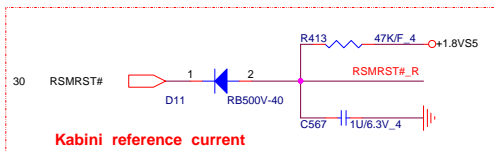
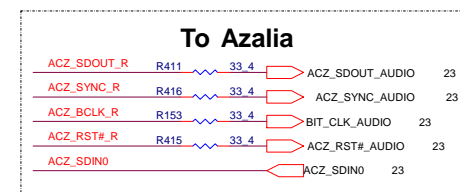
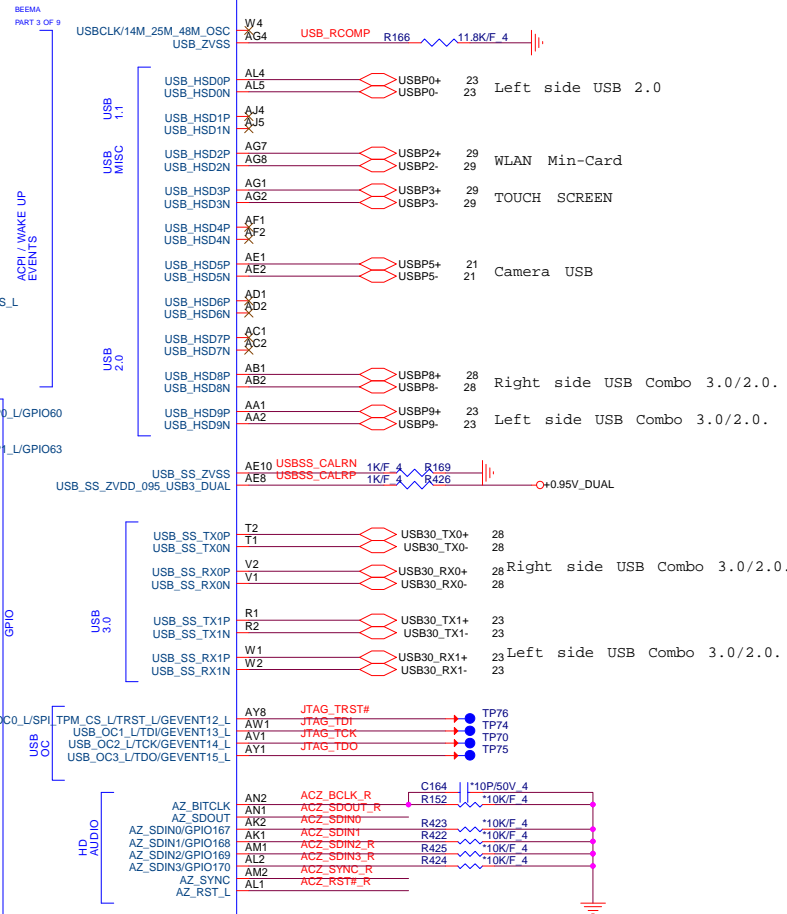
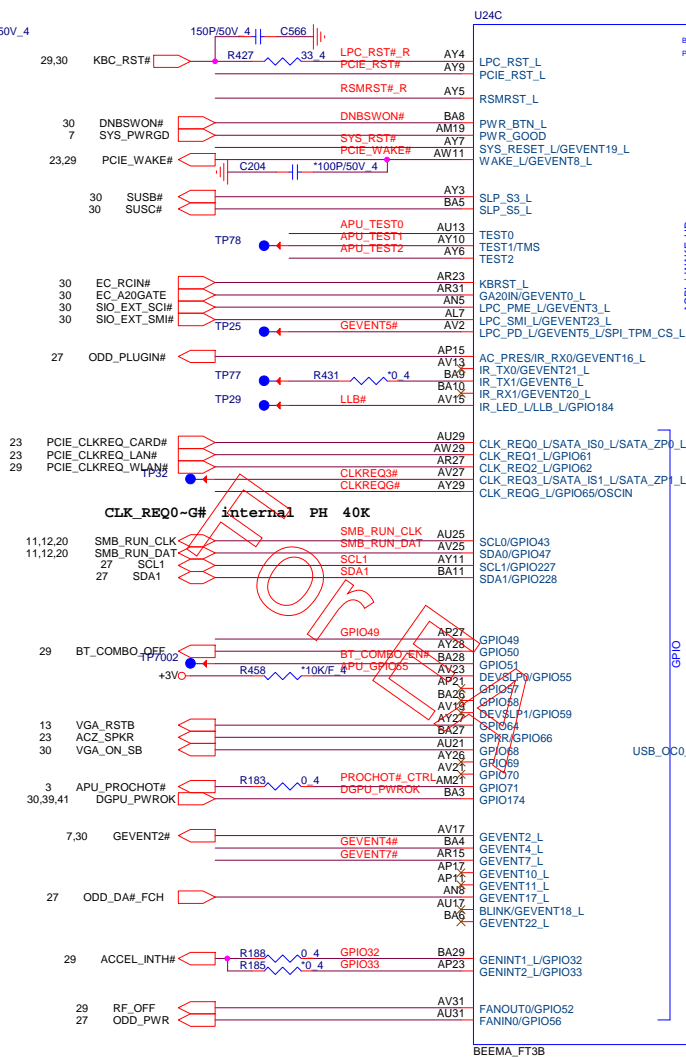
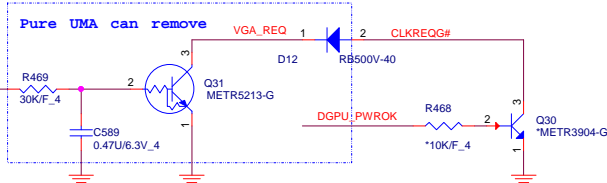
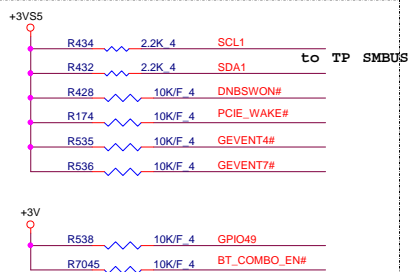
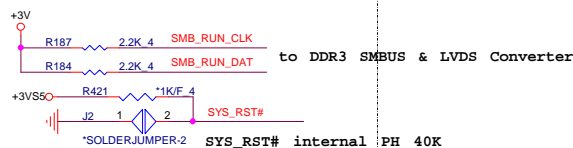
Size	Document Number	Rev
	Block Diagram	1A
Date: Tuesday, November 18, 2014 Sheet 1 of 41		

NB5/RD3



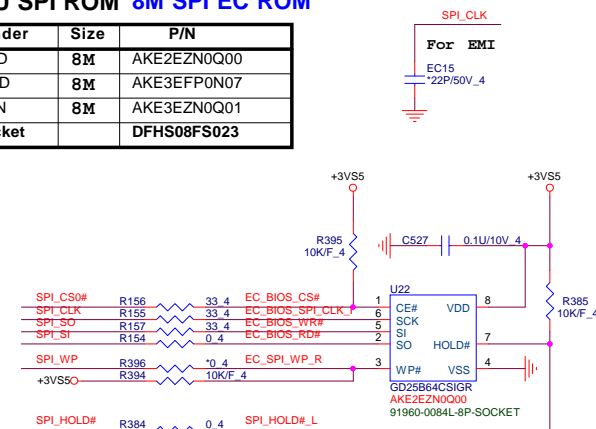


TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled





Vender	Size	P/N
GGD	8M	AKE2EZNOQ00
WND	8M	AKE3EFP0N07
EON	8M	AKE3EZNOQ01
Socket		DFHS08FS023

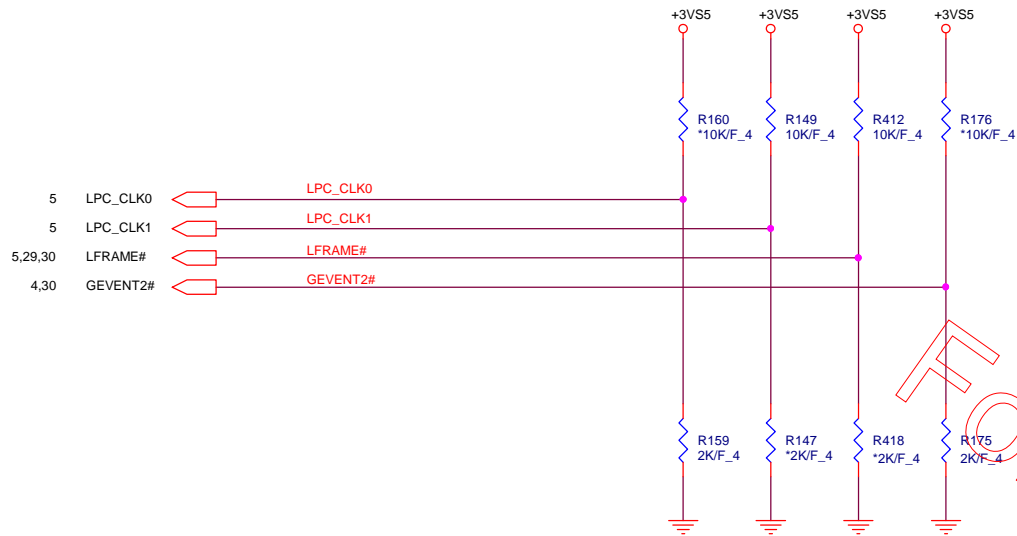




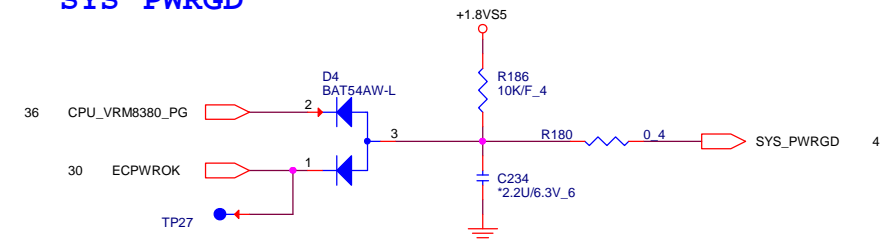


STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



SYS_PWRGD



REQUIRED STRAPS


	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT



PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
	STRAP (6/6)	1A
Date: Tuesday, November 18, 2014 Sheet 7 of 41		

For EA

	PROJECT : Y71 Quanta Computer Inc.		
	Size B	Document Number Reserved	Rev 1A
	Date: Tuesday, November 18, 2014 Sheet 8 of 41		


For EA

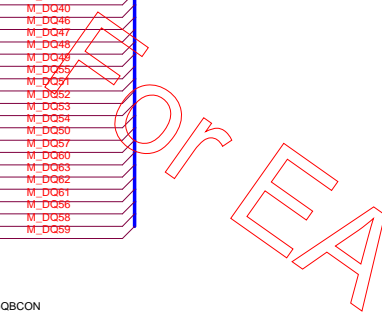


PROJECT : Y71
Quanta Computer Inc.

Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 9 of 41		

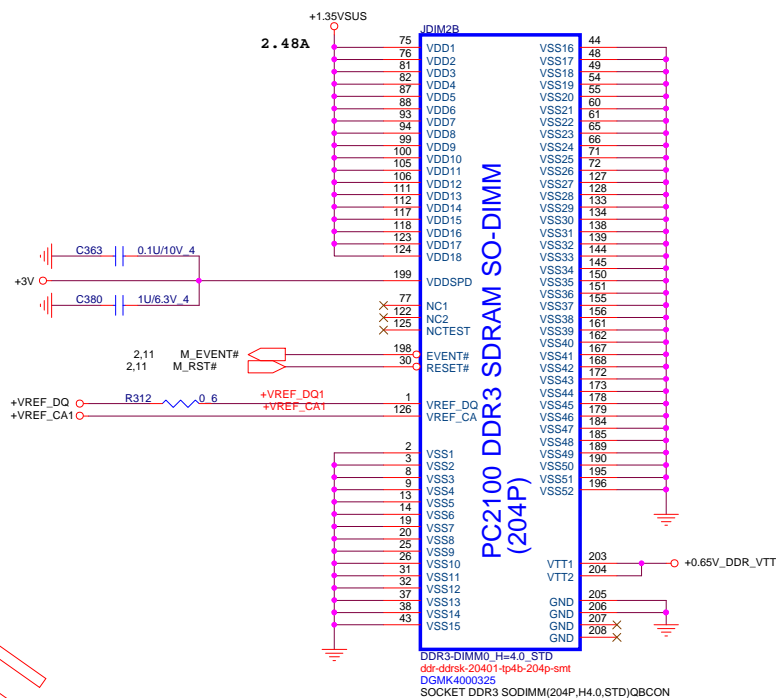
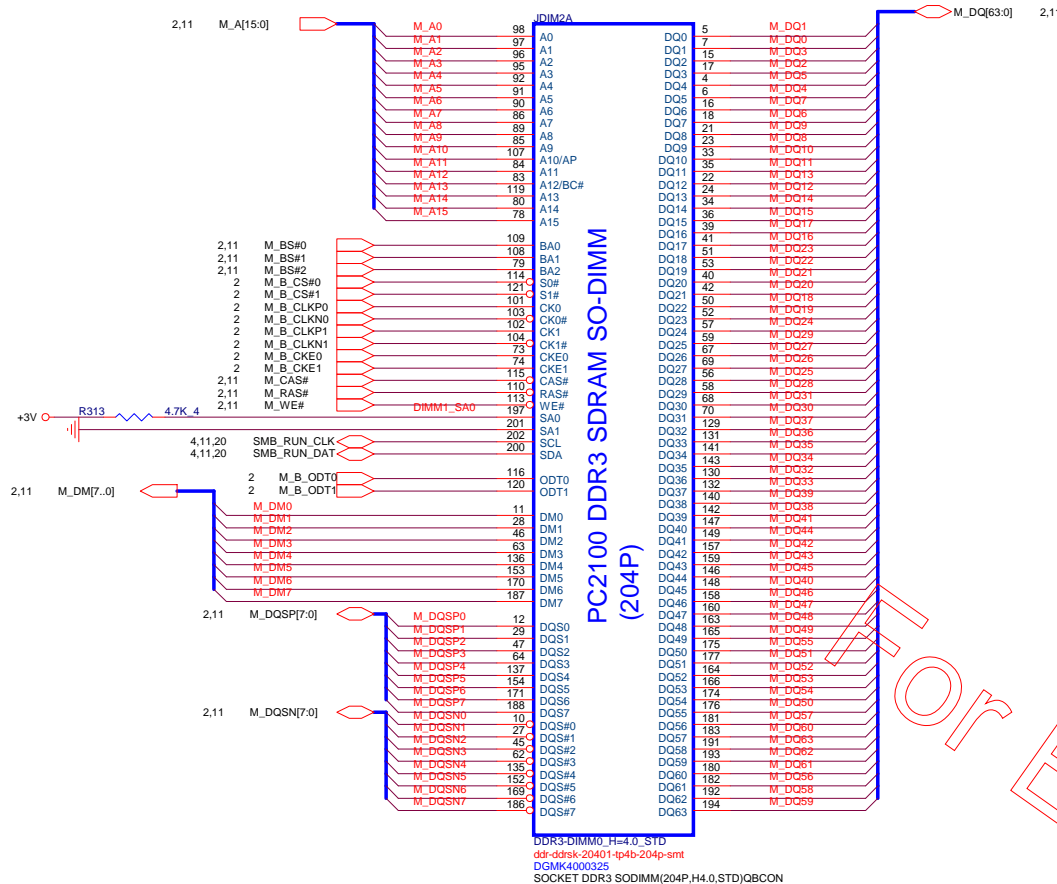
For EA

	PROJECT : Y71 Quanta Computer Inc.		
	Size B	Document Number Reserved	Rev 1A
	Date: Tuesday, November 18, 2014		Sheet 10 of 41

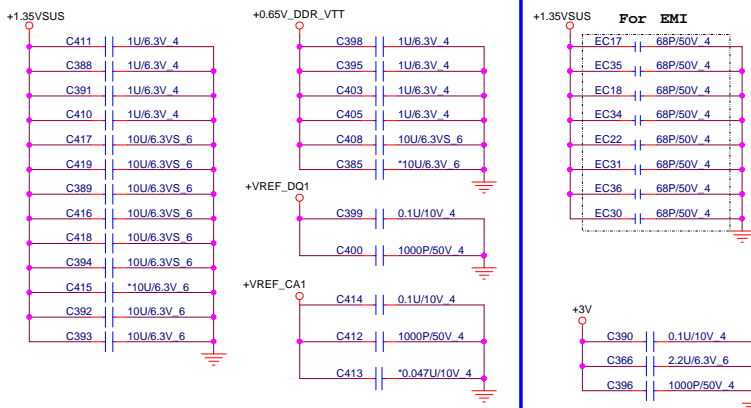


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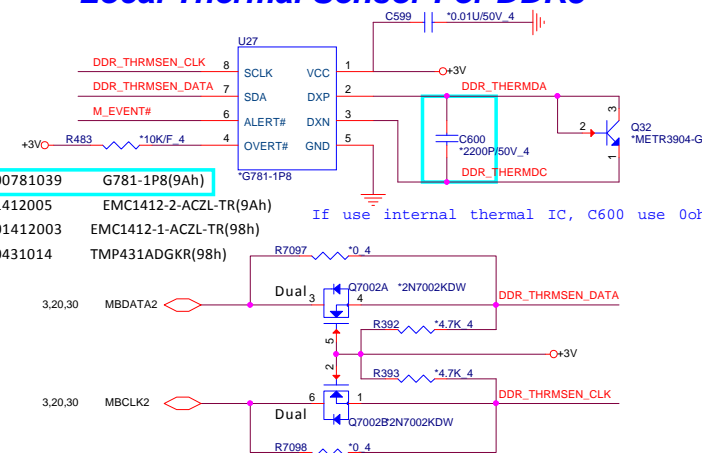


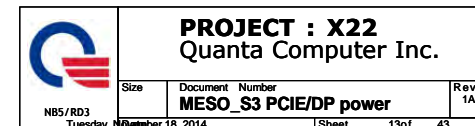


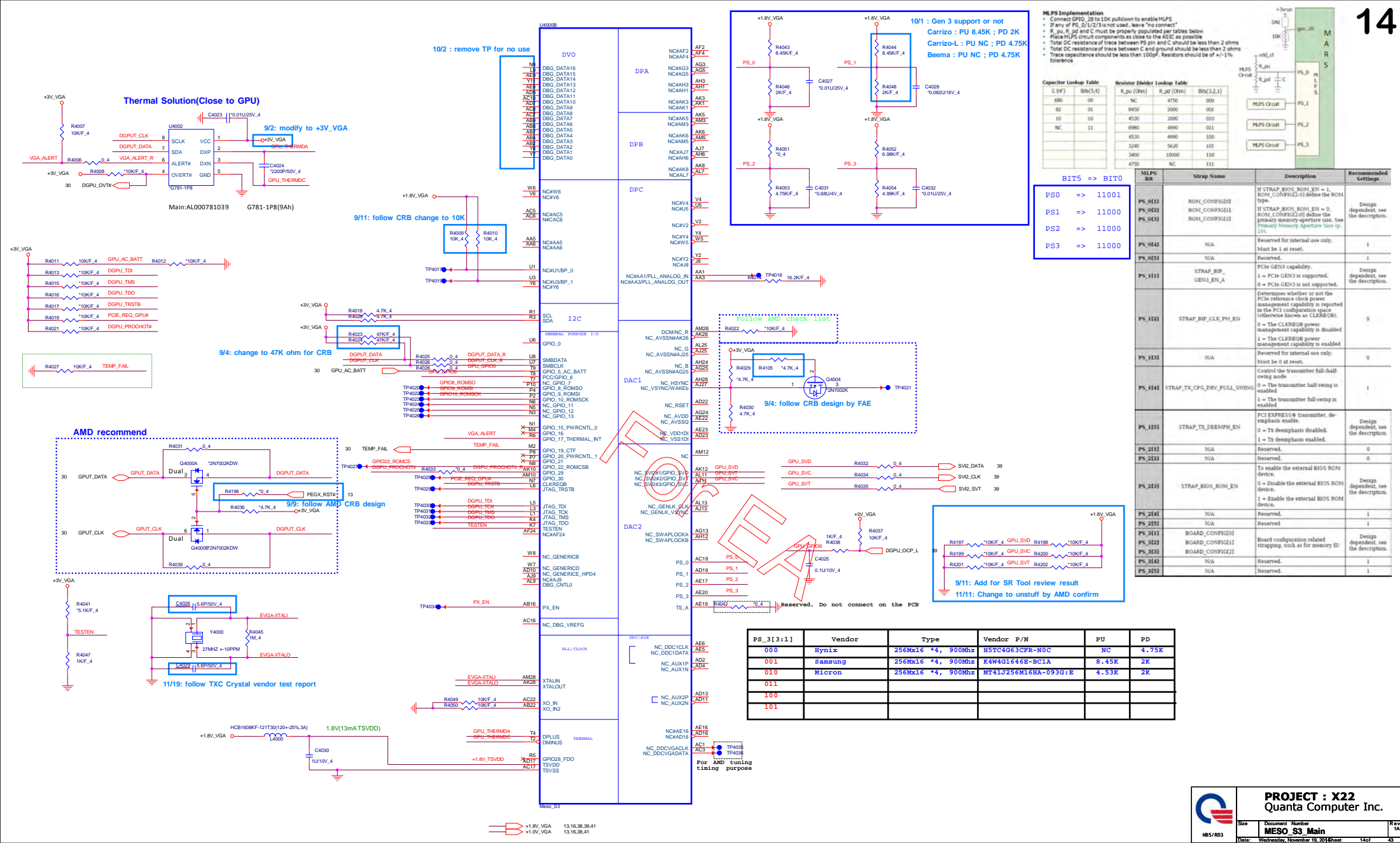
Place these Caps near So-Dimm1.

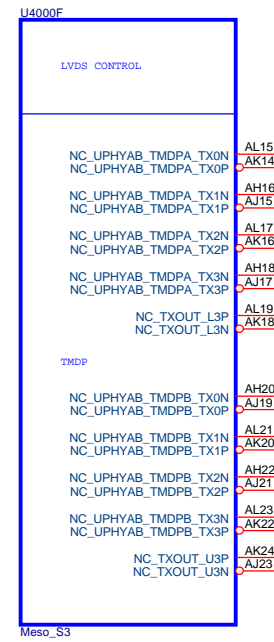
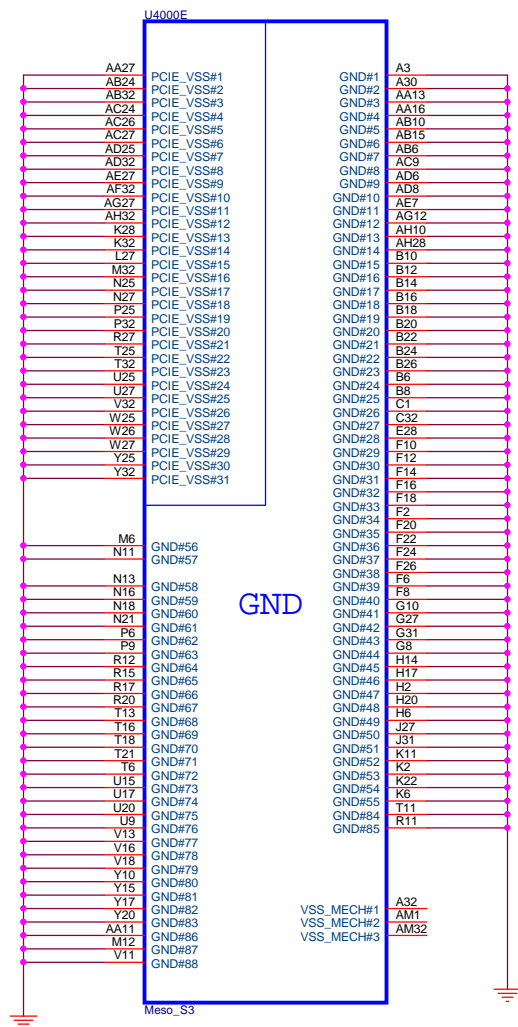


Local Thermal Sensor For DDR3









CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

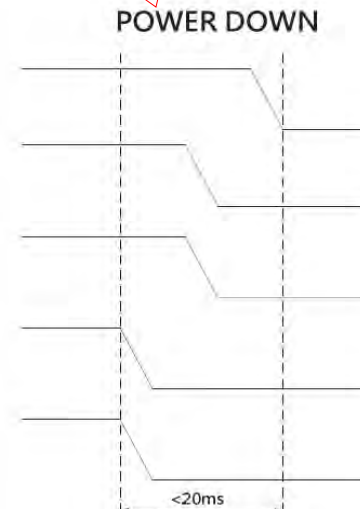
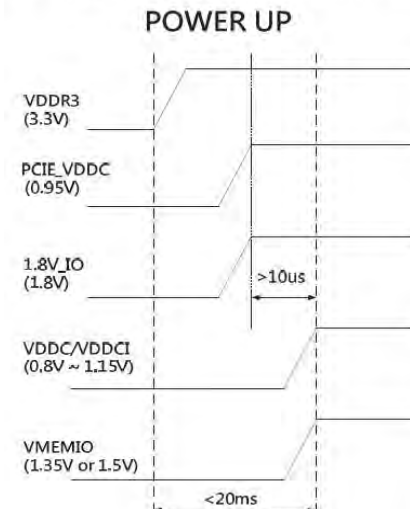
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	x
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

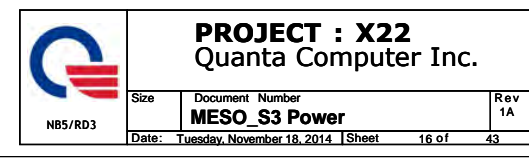
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

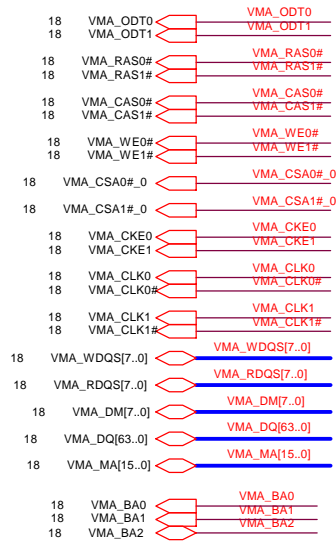
POWER UP / POWER DOWN SEQUENCE



PROJECT : X22
Quanta Computer Inc.

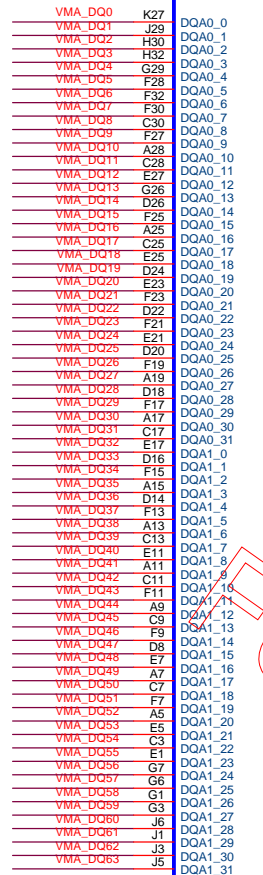
Size	Document Number	Rev
	MESO_S3_GND/LVDS/Strap	1A
Date:	Tuesday, November 18, 2014	Sheet 15 of 43



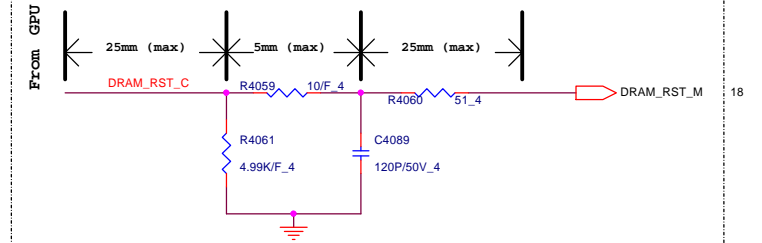
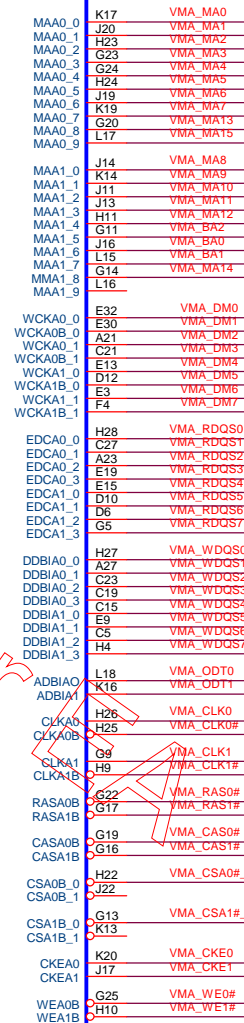


support 1Gbit
VRAM (64M x 16)

U4000C

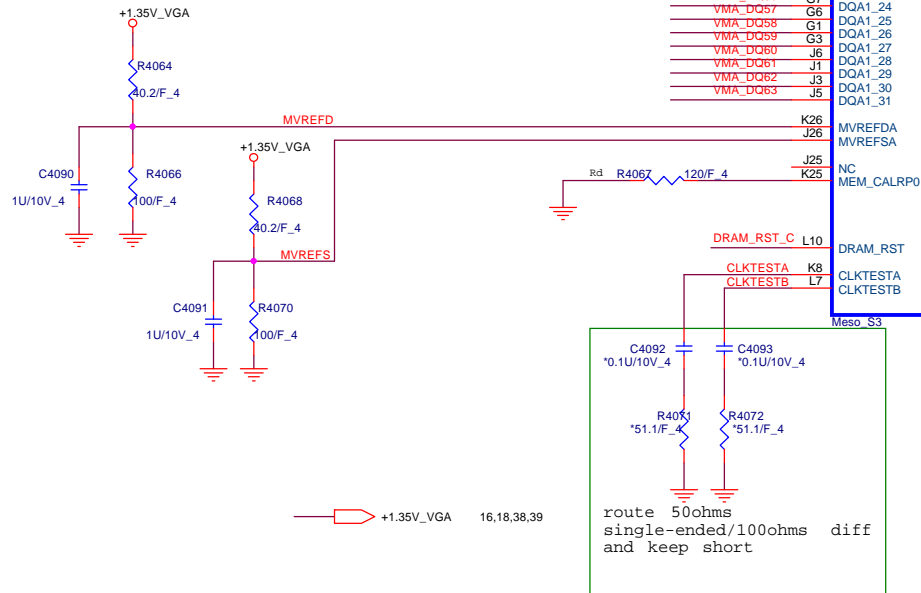


MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



→ +1.35V_VGA 16,18,38,39

route 50ohms
single-ended/100ohms diff
and keep short




NBS/RD3

PROJECT : X22
Quanta Computer Inc.

Size	Document Number	Rev
	MESO_S3_MEM_Interface	1A
Date:	Tuesday, November 18, 2014	Sheet 17 of 43



FOR EA

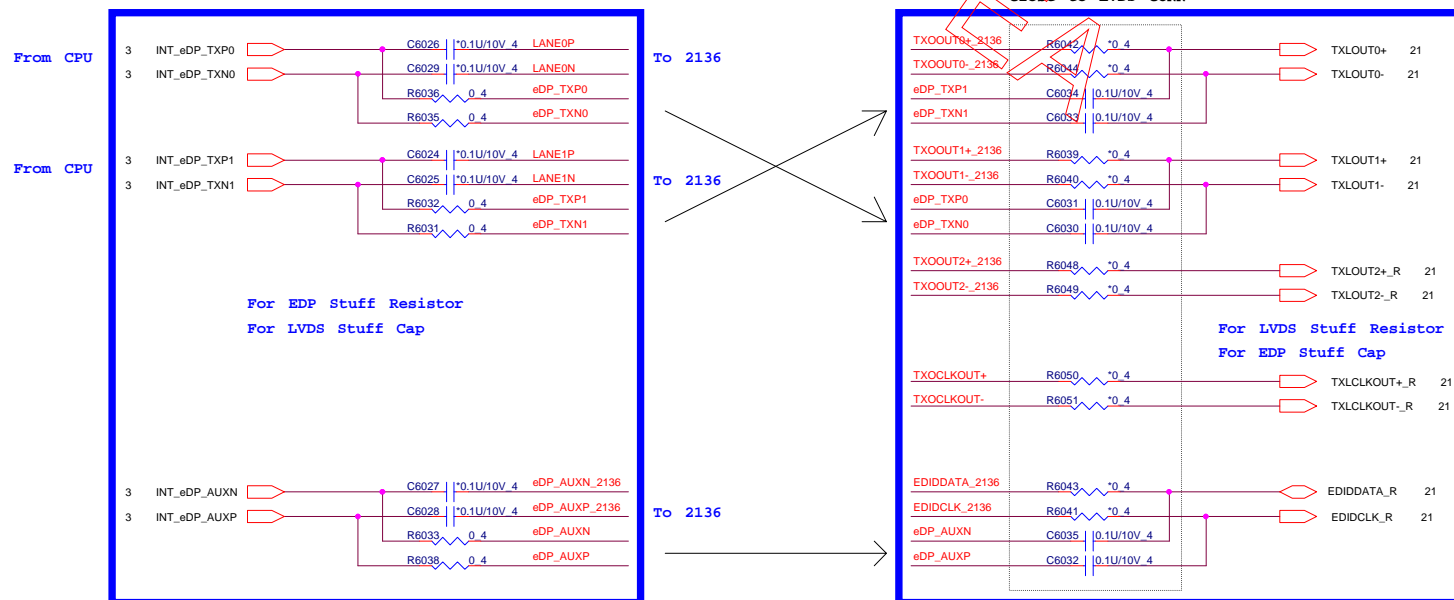
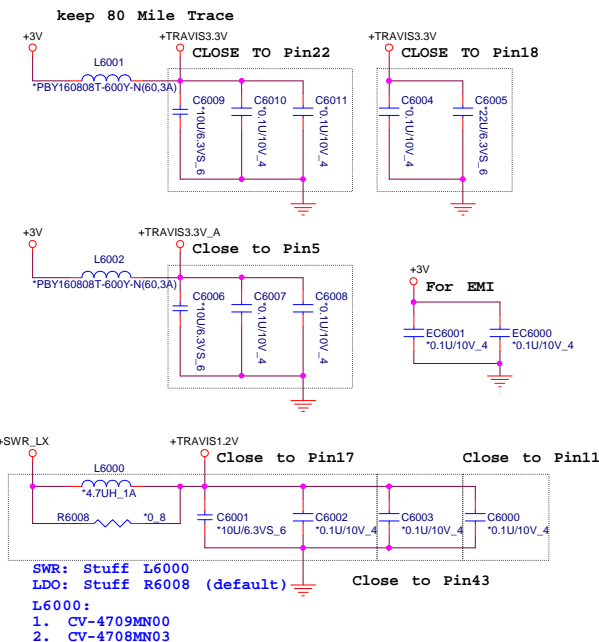
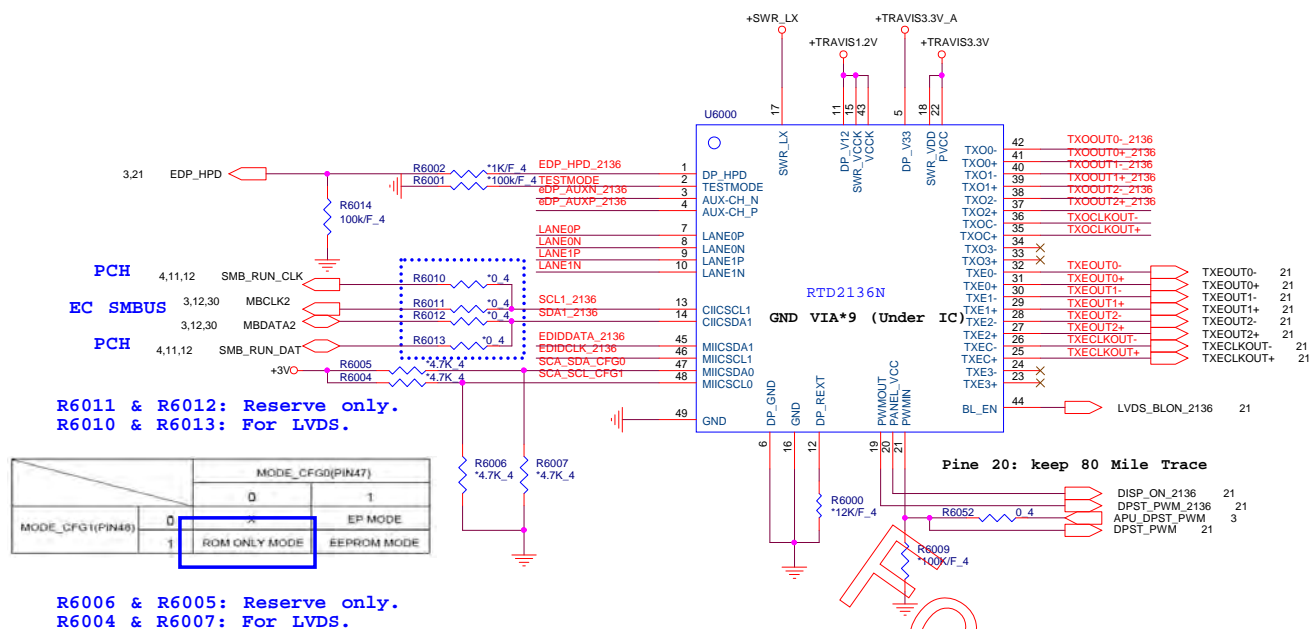


NBS/RD3

PROJECT : X22
Quanta Computer Inc.

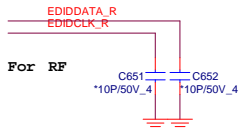
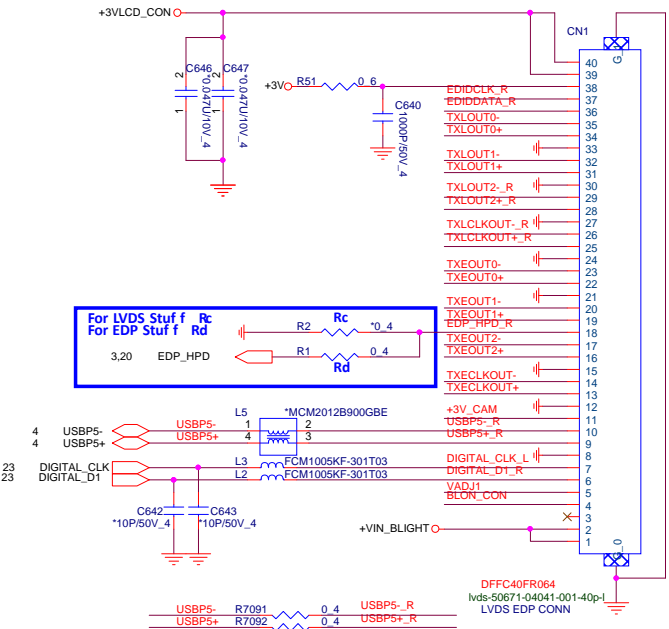
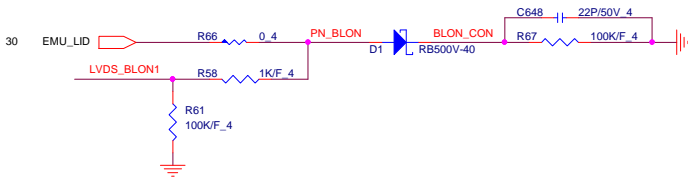
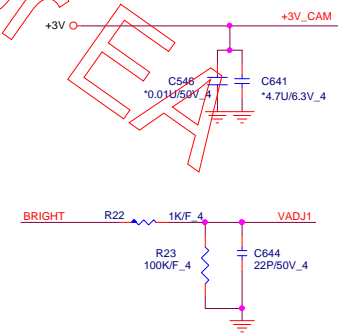
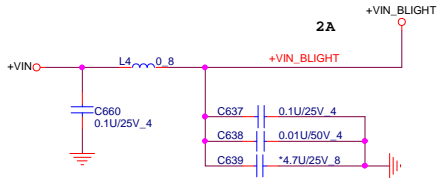
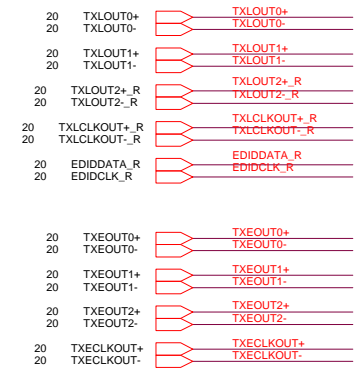
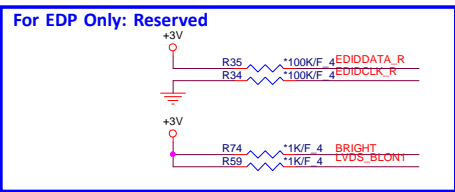
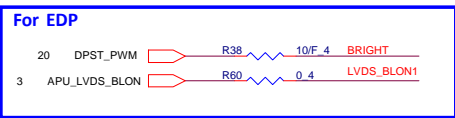
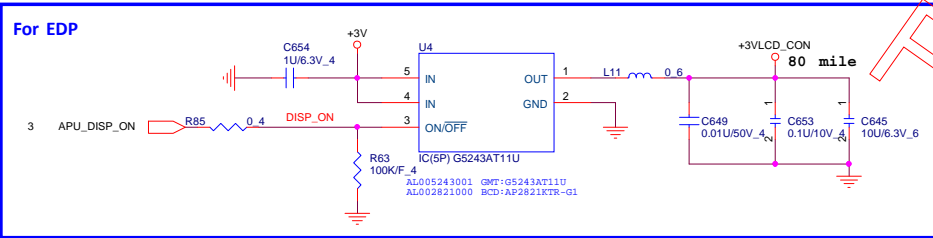
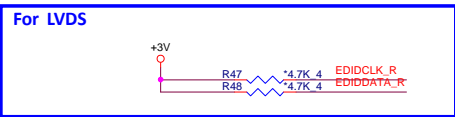
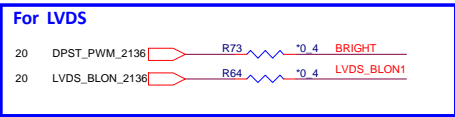
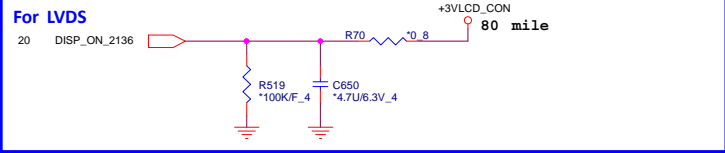
Size Custom	Document Number MESO S3 VRAM(DDR3 BGA96P)	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 1801 43		

Pine 15/17: keep 20 Mile Trace
Pine 18: keep 80 Mile Trace



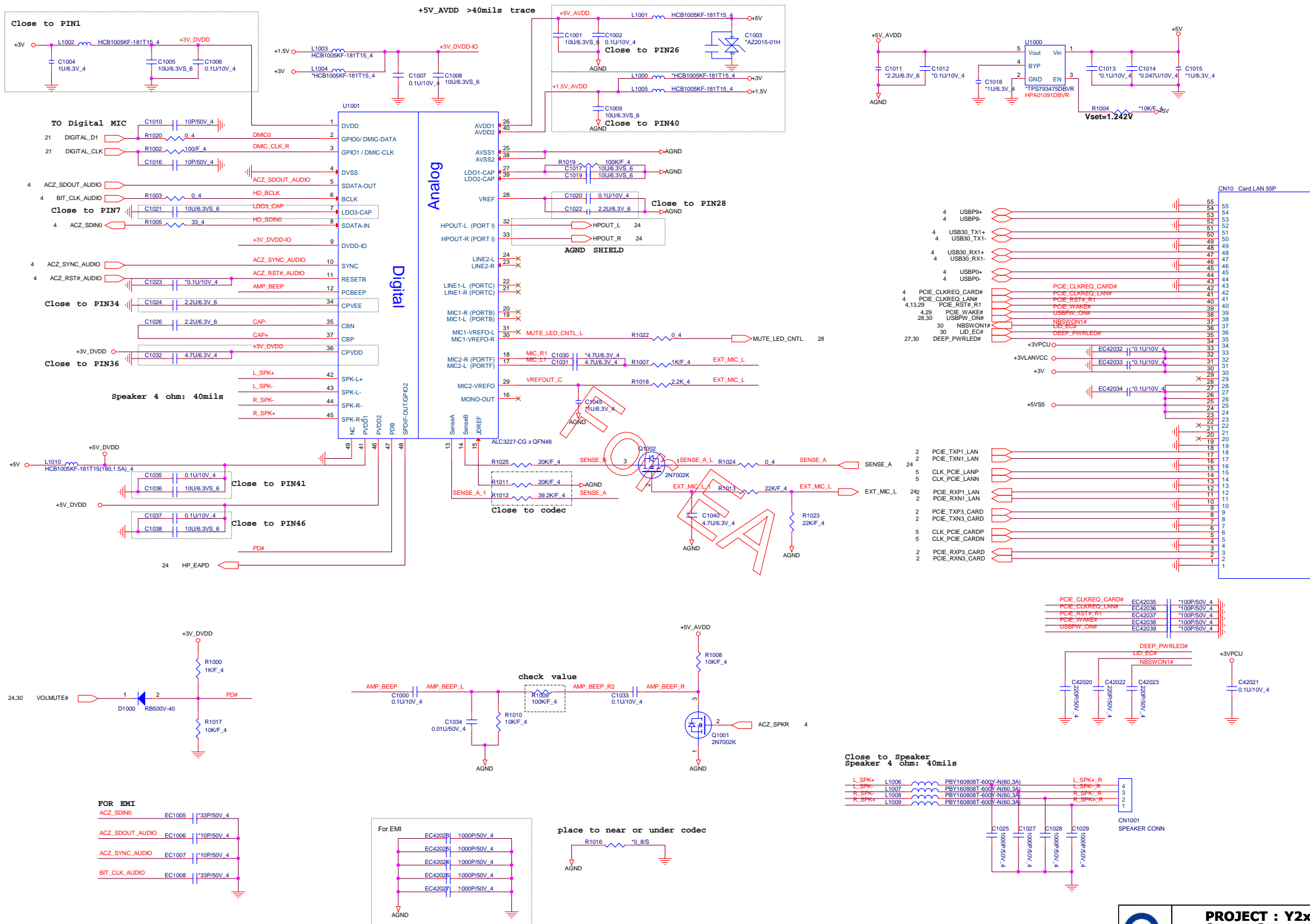
LVDS CONN.

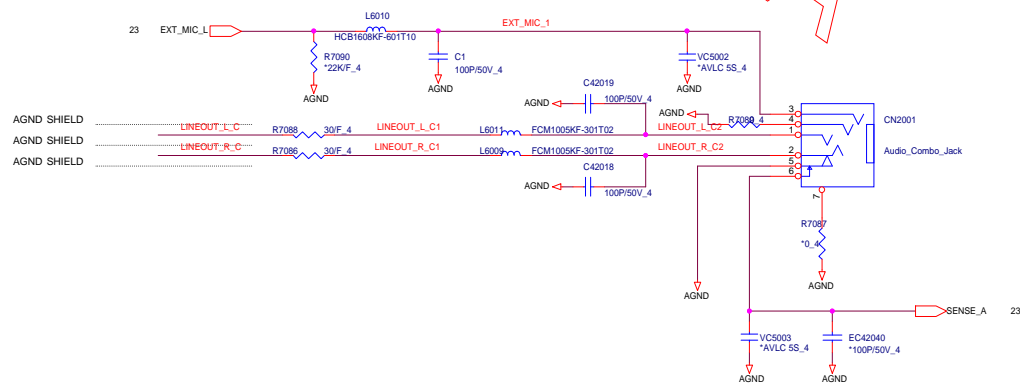
Note.
14" & 15" only eDP panel.
17" have both LVDS & eDP panel.



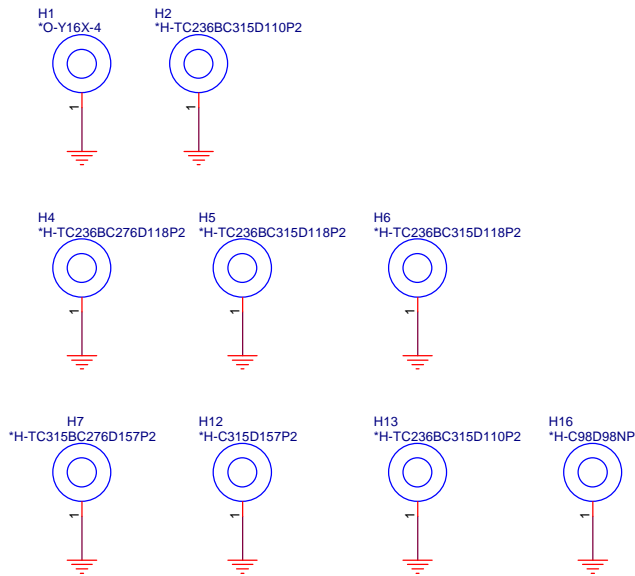


Size B	Document Number HDMI	Rev 1A
Date: Tuesday, November 18, 2014		Sheet 22 of 41

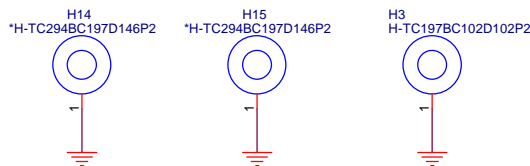




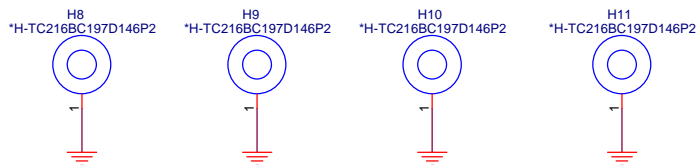
Holes



GPU HOLES

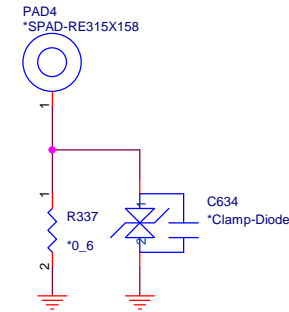


APU HOLES

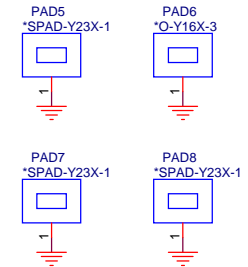


WLAN NUT

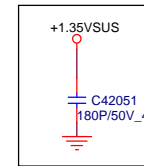
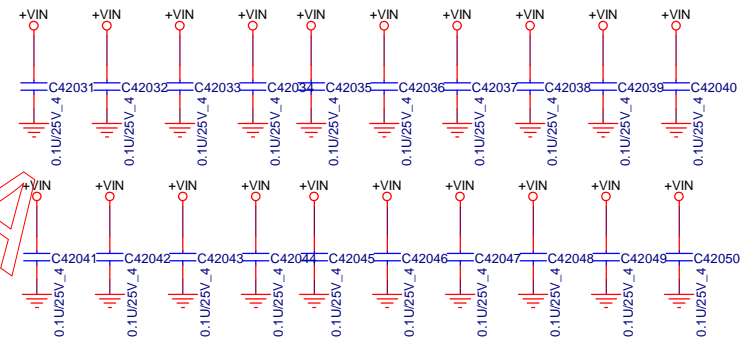
Metal ESD




EMI




Place on +VIN path



11/17 EMI request

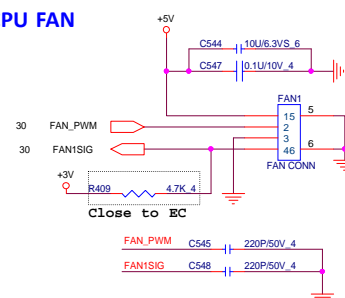
 NB5/RD3	PROJECT : Y2x Quanta Computer Inc.		
	Size B Document Number Holes / EMI	Date: Tuesday, November 18, 2014	Sheet 25 of 41 Rev 1A

For EA

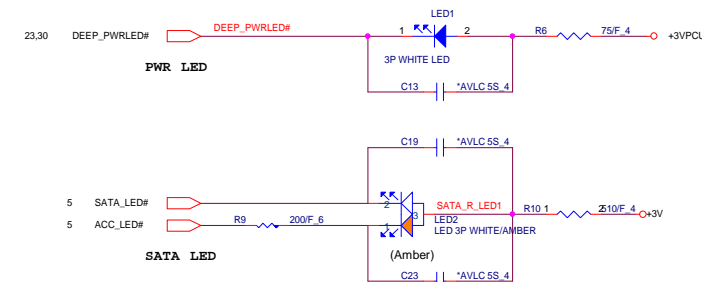
 NB5/RD3	PROJECT : Y2x Quanta Computer Inc.		
	Size B	Document Number Reserved	Rev 1A
	Date: Tuesday, November 18, 2014 Sheet 26 of 41		

Power But t on Connect or (Momet o DB)

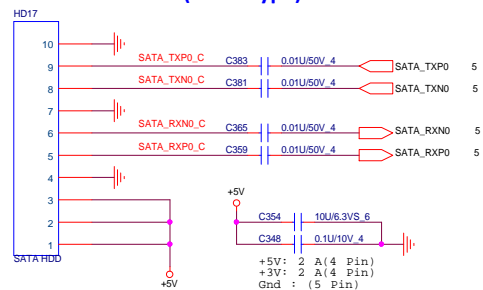
CPU FAN



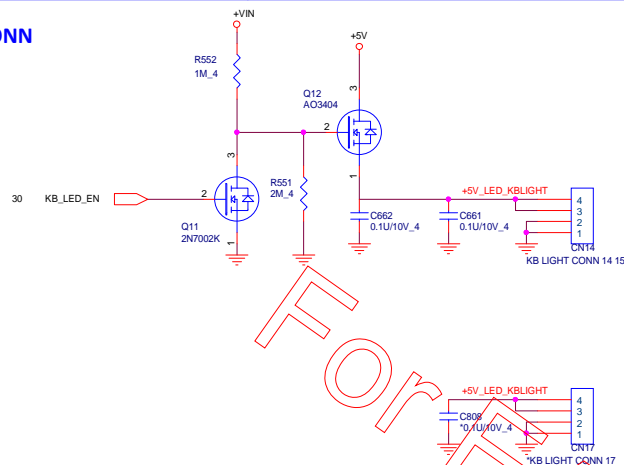
LED



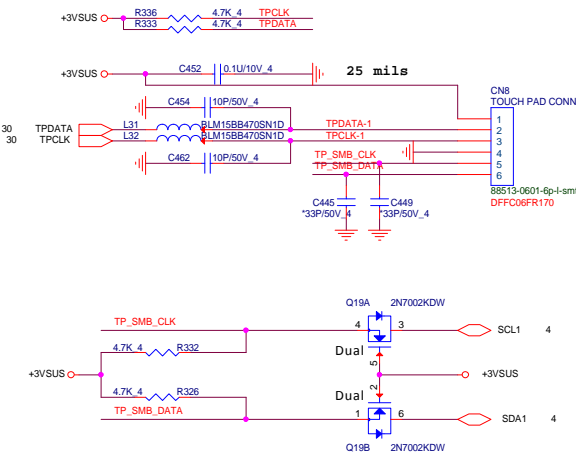
SATA HDD CONN (Cable type)



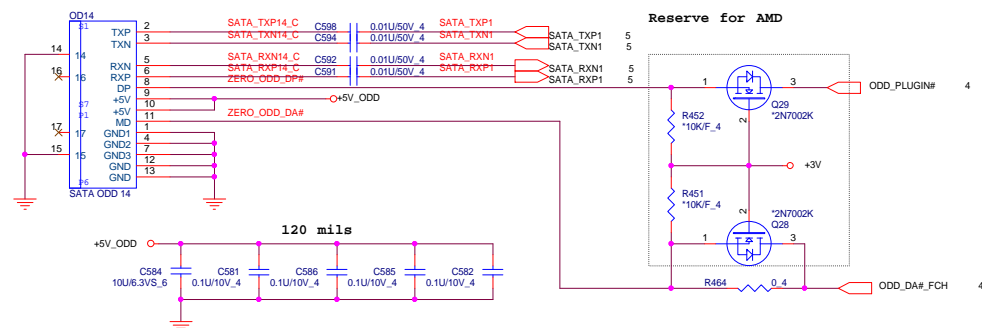
KB LIGHT CONN



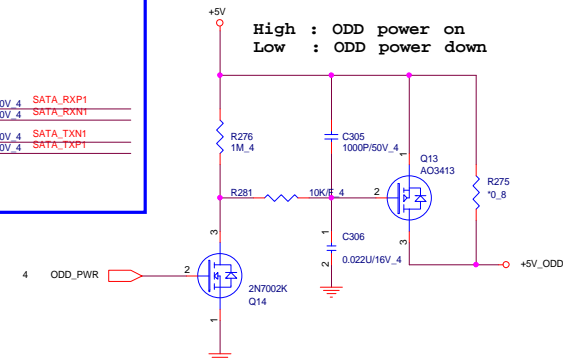
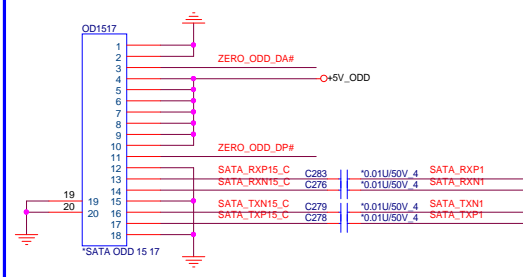
Touch Pad



14" SATA ODD CONN

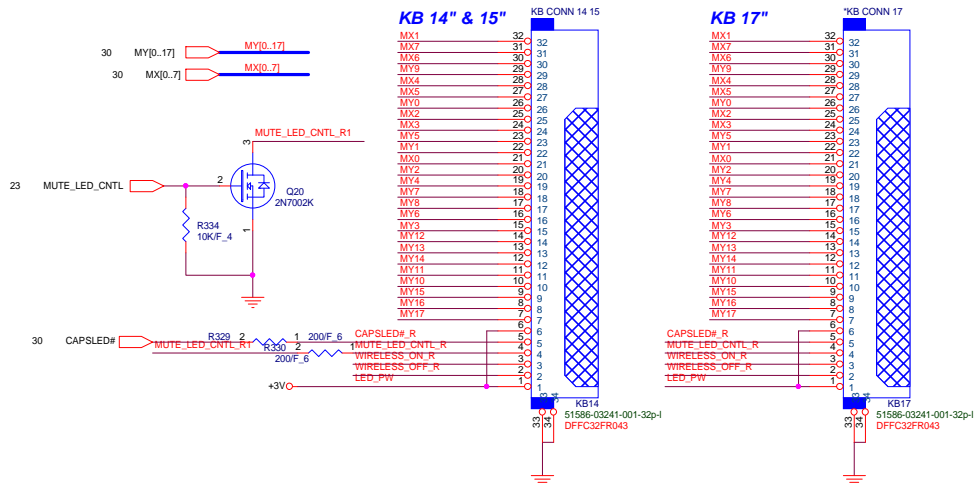


15" & 17" SATA ODD CONN

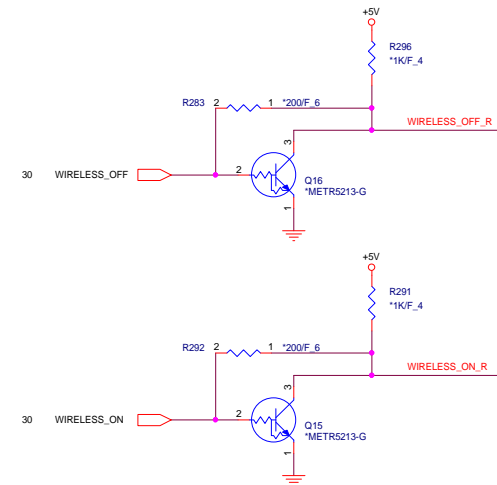
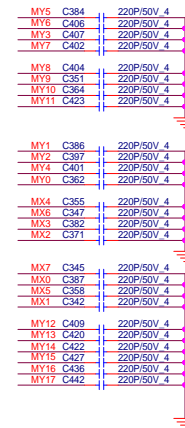
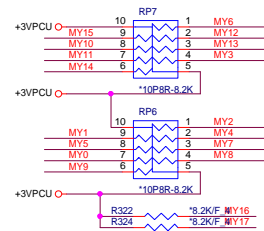


PROJECT : Y2x
Quanta Computer Inc.

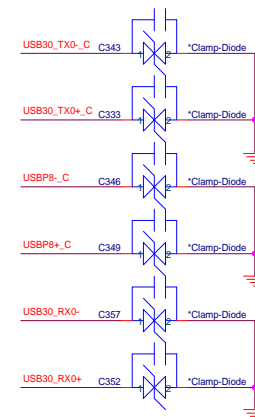
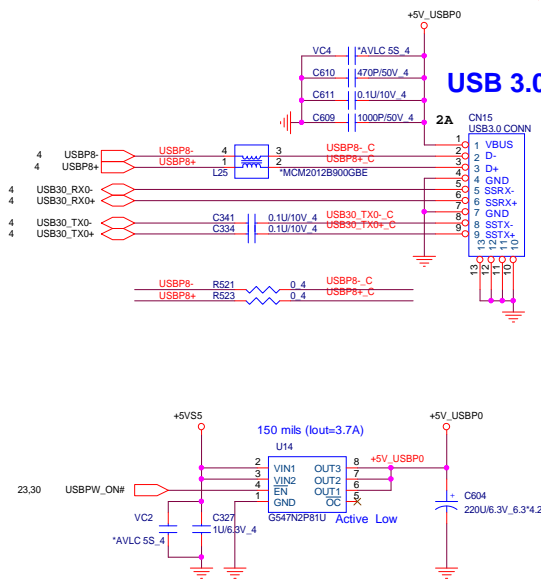
Size	Document Number	Rev
Custom	HDD/ODD/TP/FAN/LID/LED	1A
Date: Tuesday, November 18, 2014	Sheet 27 of 41	



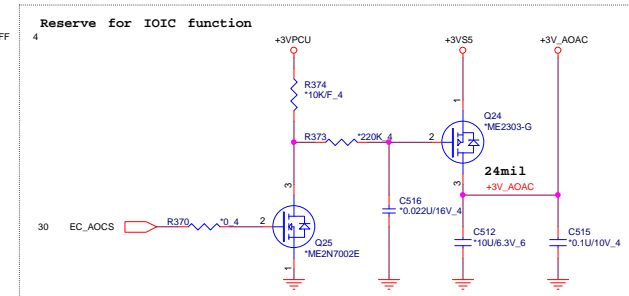
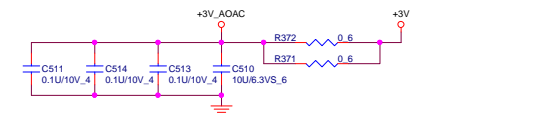
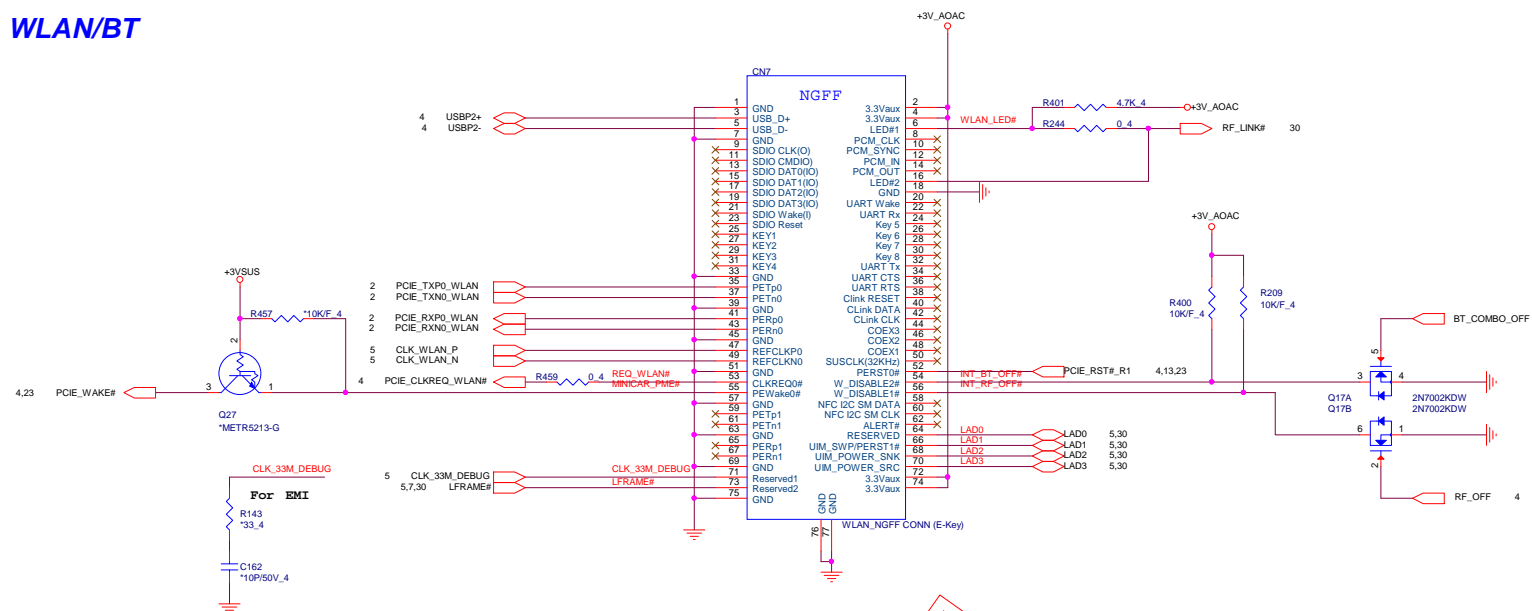
KEYBOARD PULL-UP



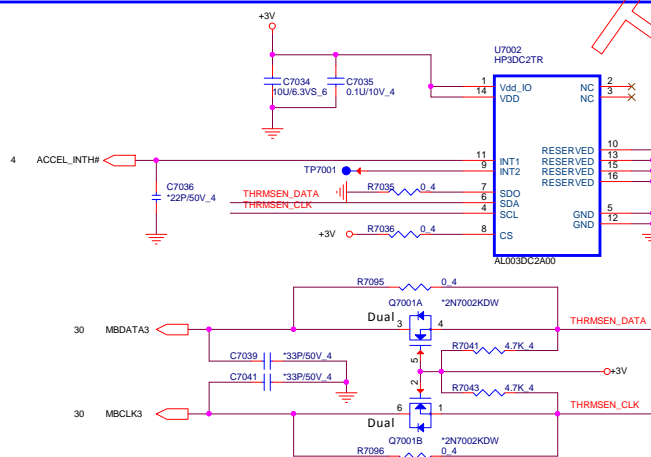
Left USB 2.0/3.0 Combo



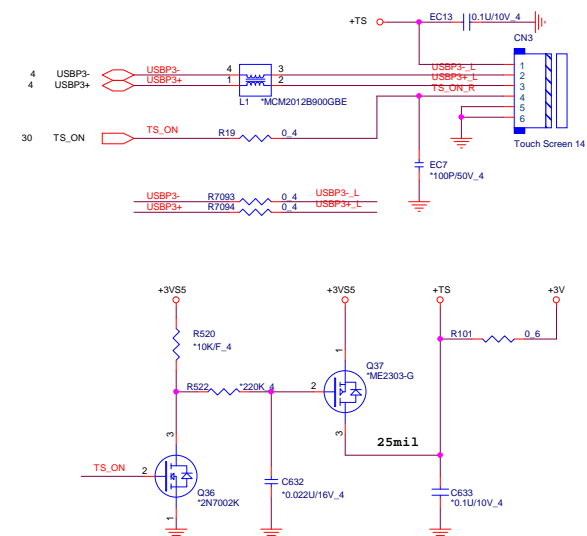
WLAN/BT



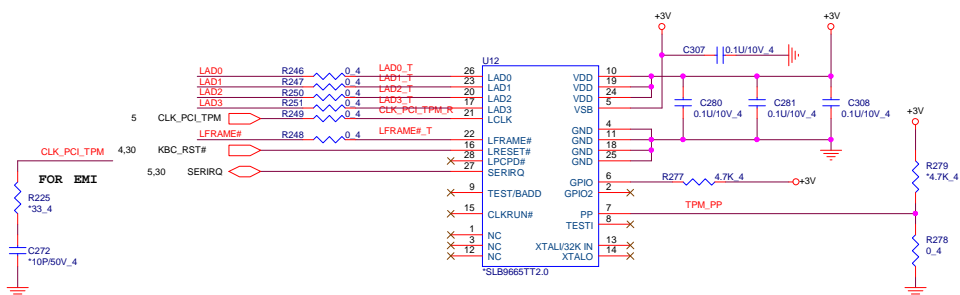
Accelerometer Sensor

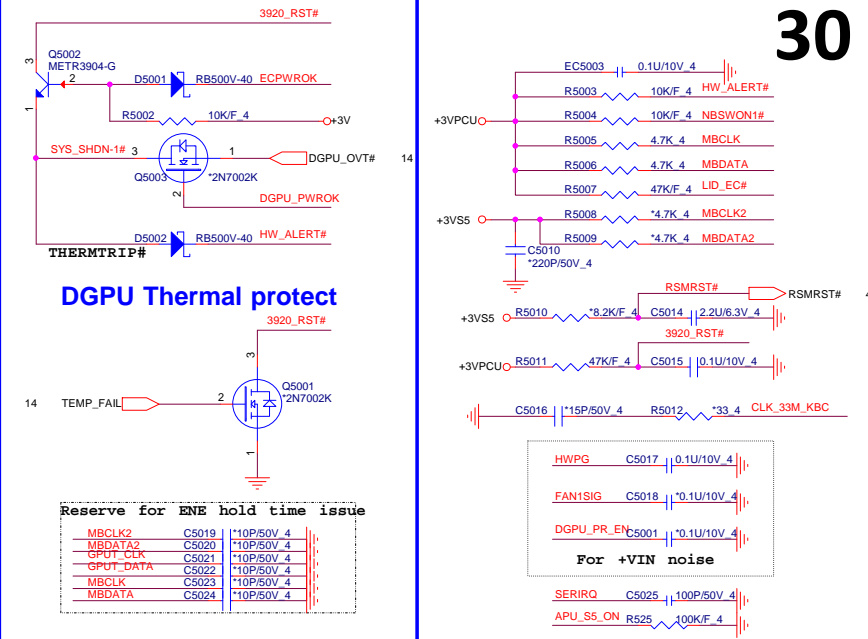
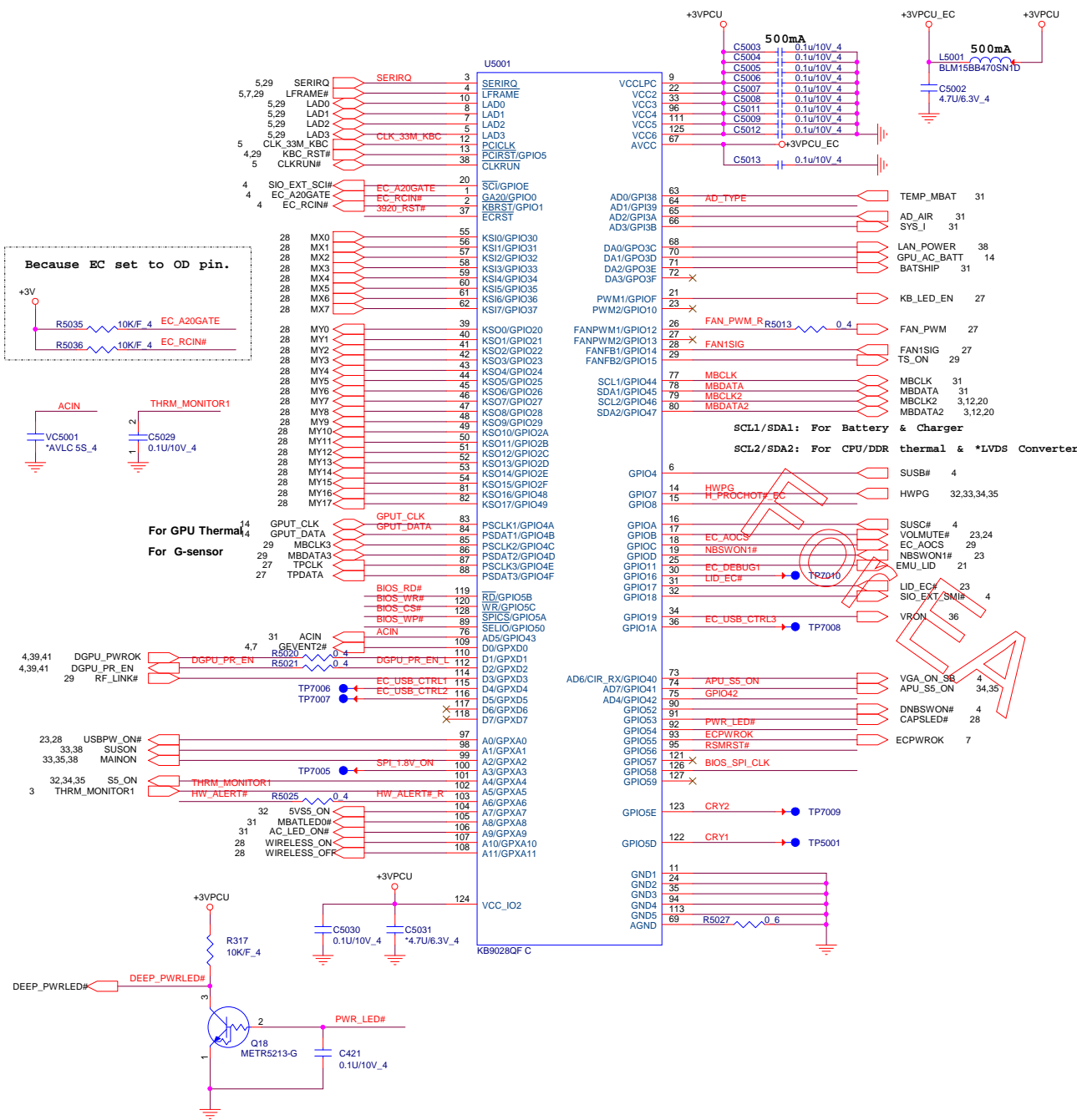


Touch screen

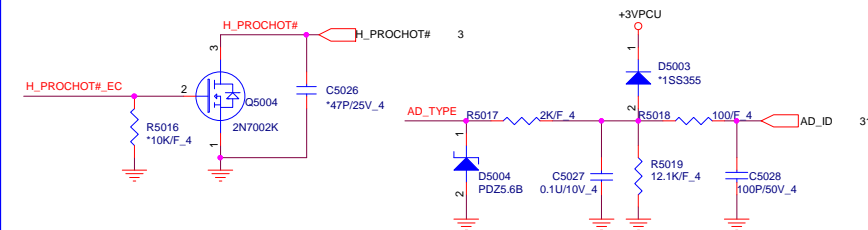


TPM (2.0)

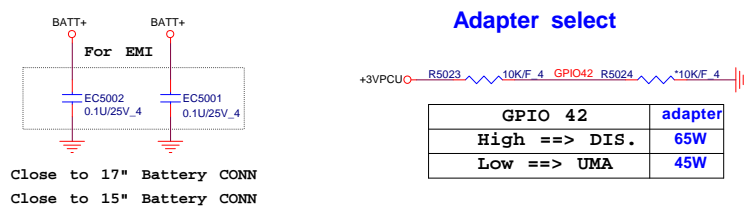




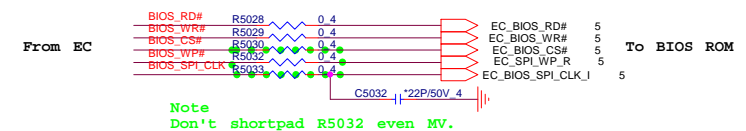
Smart adapter Type check




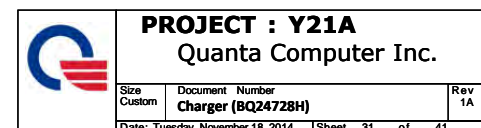
Adapter select



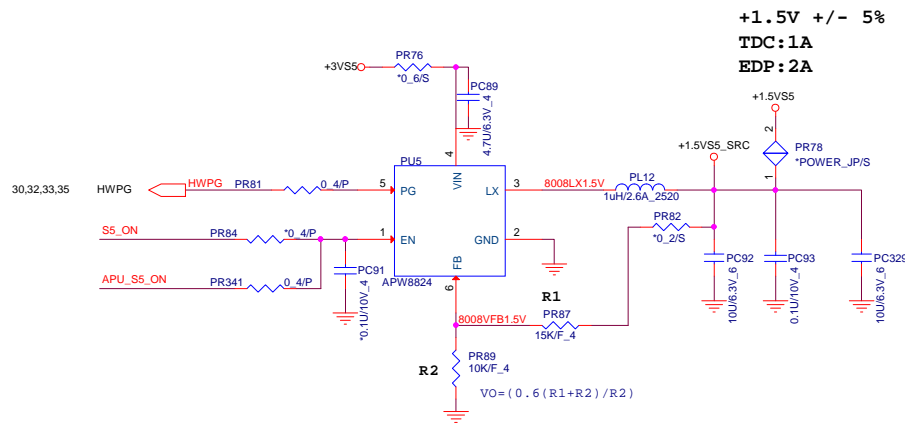
SPI SIGNALS



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NB5/RD3	Date: Tuesday, November 18, 2014	Sheet 30 of 41	



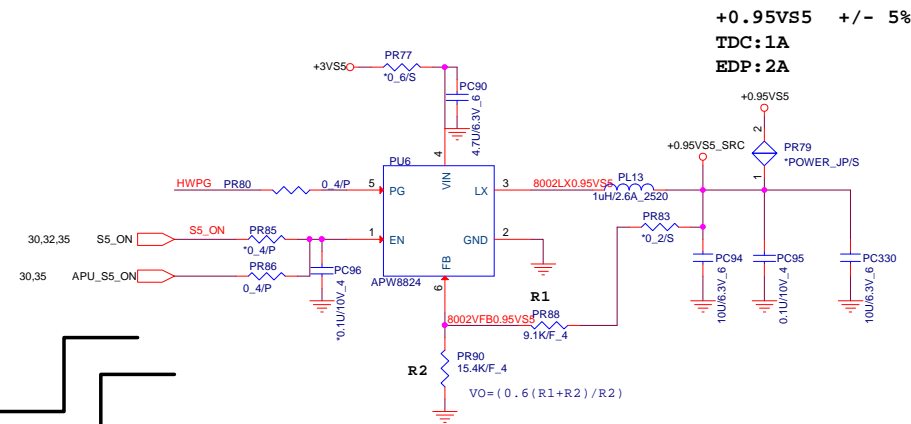





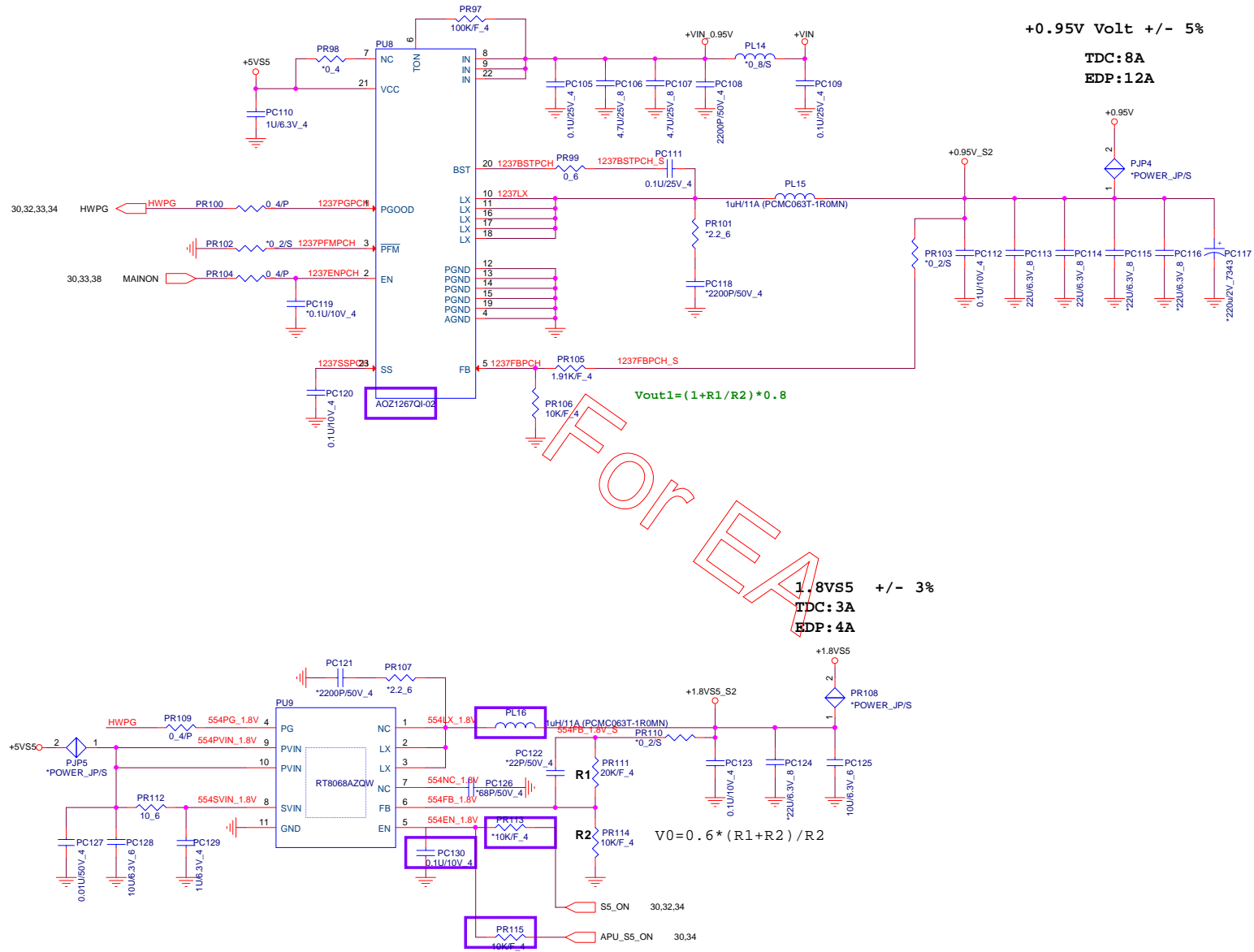
S5_ON

APU_S5_ON

FOR EA

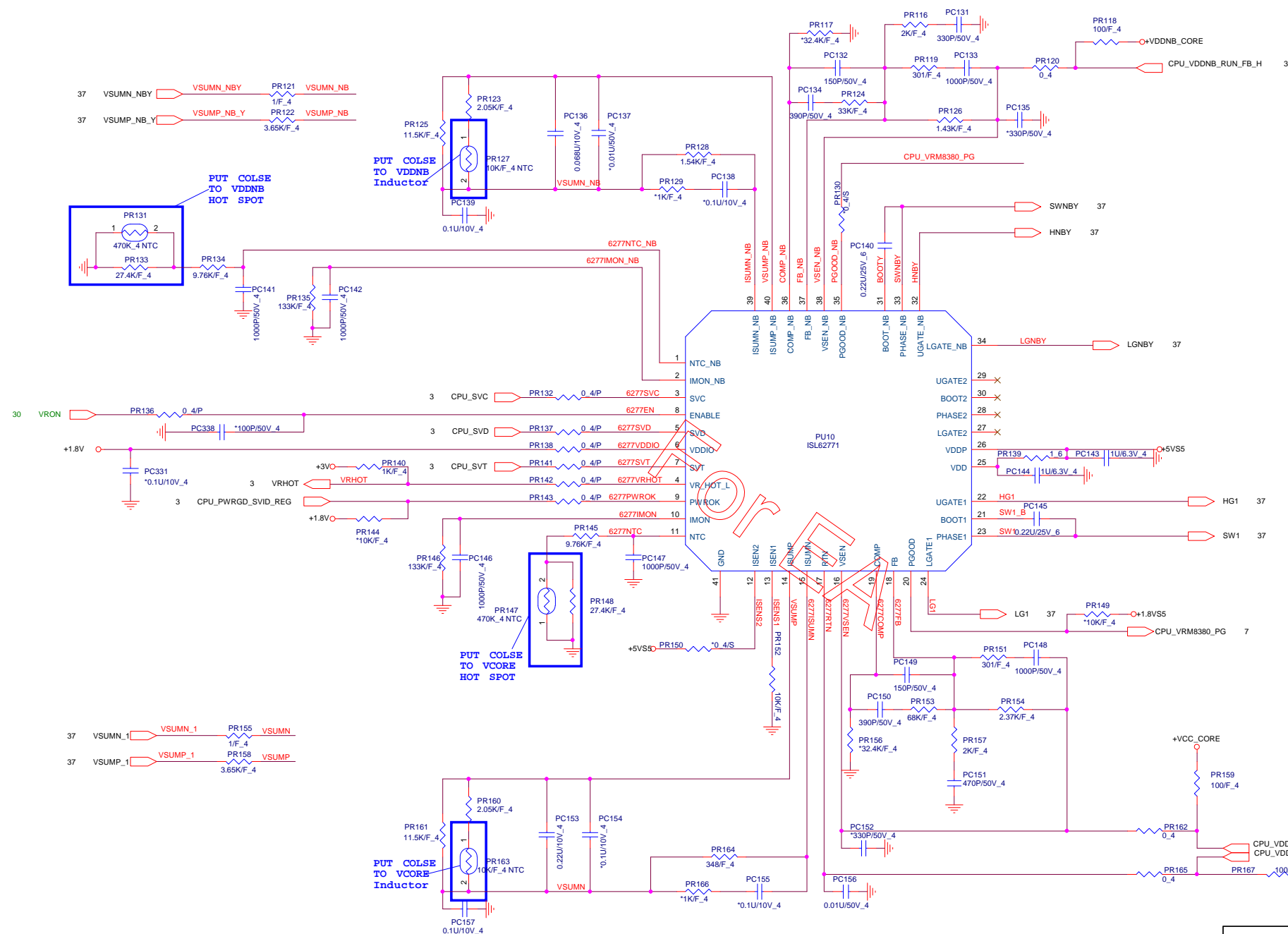


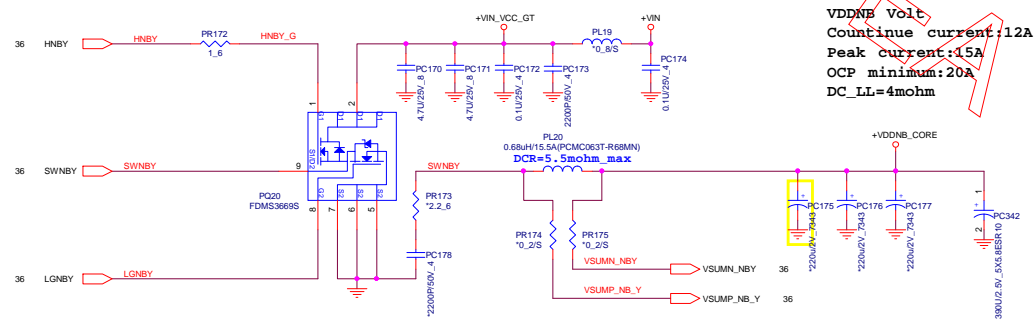
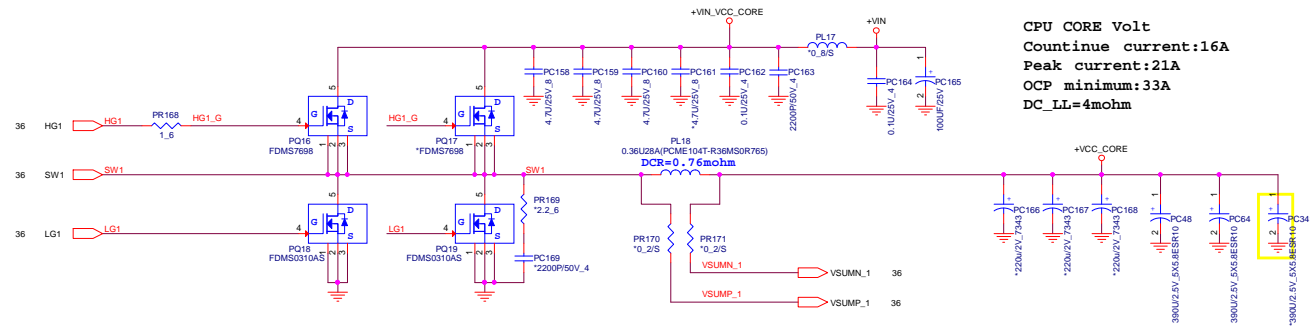
 PROJECT : Y21A Quanta Computer Inc.		
Size Custom	Document Number +1.1VS5 (RT8228)/2.5V	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 34 of 41		

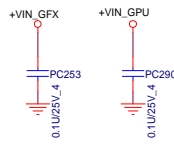
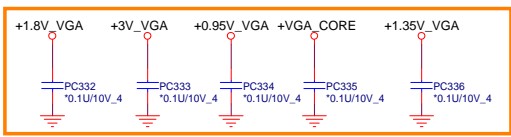


PROJECT : Y21A
Quanta Computer Inc.

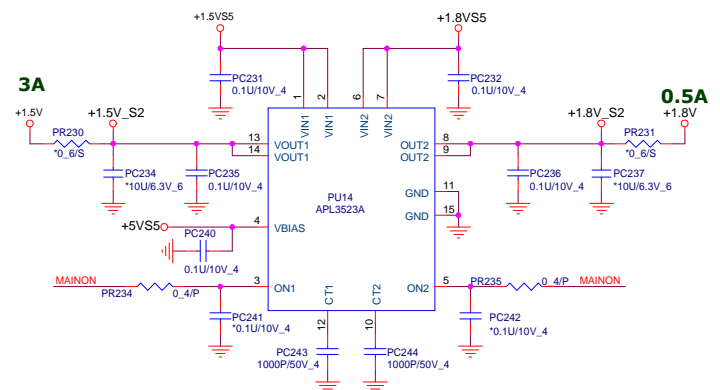
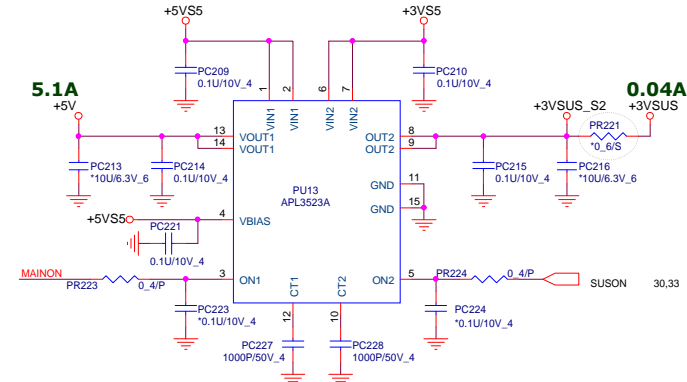
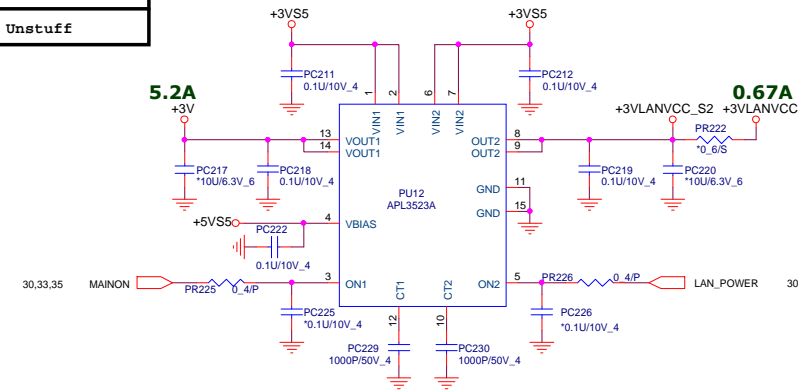
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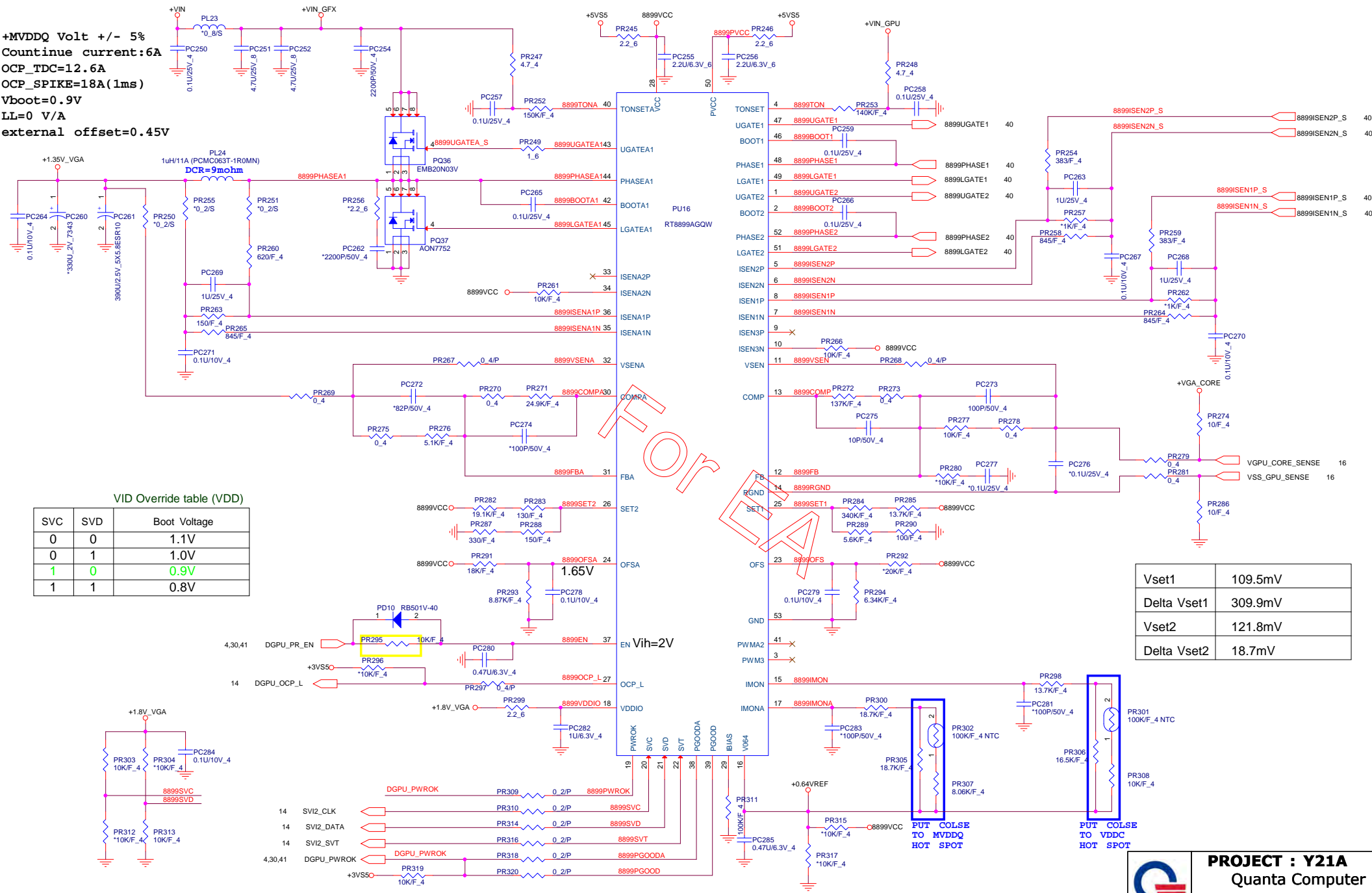


UMA only	Stuff
discrete	Unstuff




FOR EA

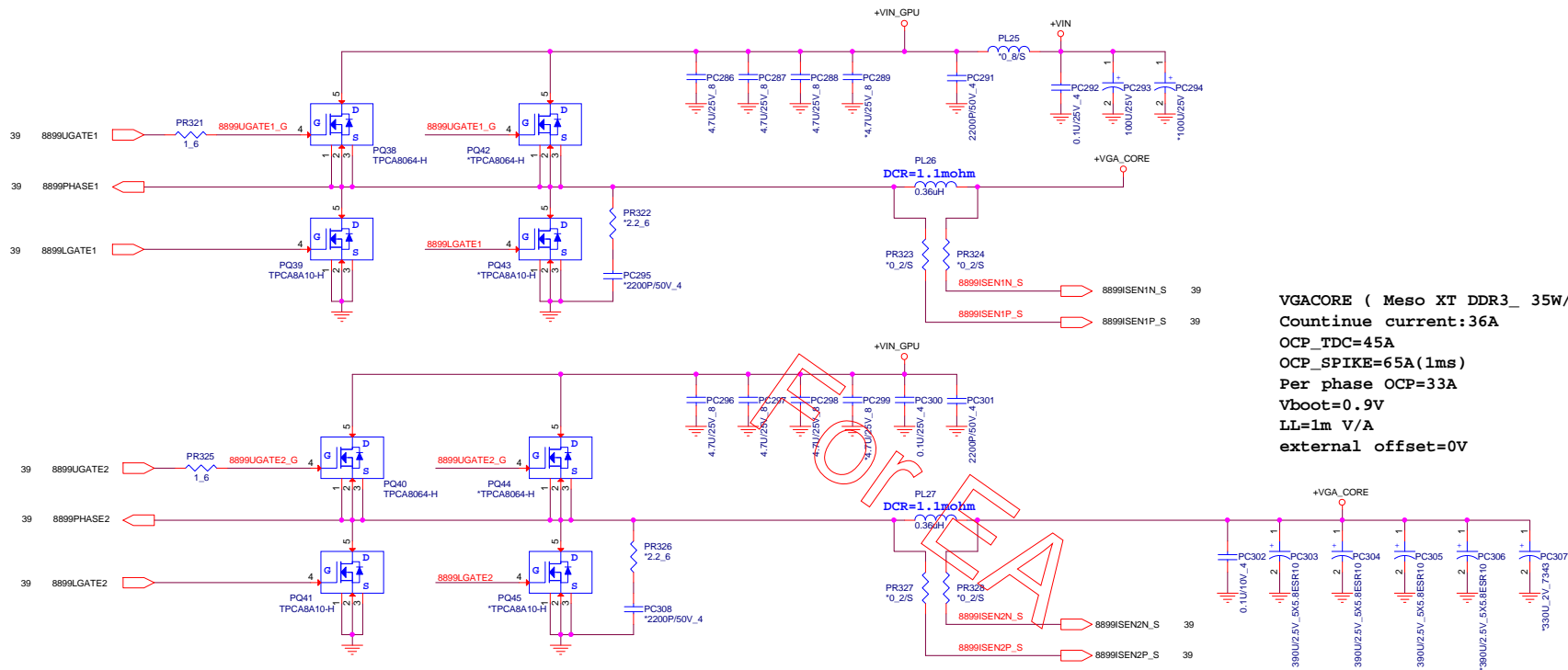
```
+MVDDQ Volt +/- 5%
Continue current:6A
OCP_TDC=12.6A
OCP_SPIKE=18A(1ms)
Vboot=0.9V
LL=0 V/A
external offset=0.45V
```




SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV

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VGACORE (Meso XT DDR3_ 35W/53W(1ms))
 Countinue current:36A
 OCP_TDC=45A
 OCP_SPIKE=65A(1ms)
 Per phase OCP=33A
 Vboot=0.9V
 LL=1m V/A
 external offset=0V

		PROJECT : Y21A	
		Quanta Computer Inc.	
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